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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,416	11/01/2001	William John Goetzinger	ROC920010204US1	2592

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EXAMINER
MERED, HABTE

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,416	GOETZINGER ET AL.	
	Examiner	Art Unit	
	Habte Mered	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 01 November 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1-4, and 19** are rejected under 35 U.S. C. 102(e) as being anticipated by Chao et al (US 6, 081, 507), hereinafter referred to as Chao.

Chao teaches methods and apparatus for handling time stamp aging. Chao teaches how time stamp aging is detected and consequently marking the obsolete time stamp for purging in systems employing fair packet queuing algorithms.

3. Regarding **claims 1 and 19**, Chao discloses a scheduling method for implementing Quality-of-Service (QoS) scheduling of a plurality of flows **(Column 1, Lines 15-20)** with aging time stamps **(Column 18, Lines 28-42)** comprising the steps of:

sequentially accessing a subset of time stamp data from a time stamp aging memory array; each time stamp data subset containing time stamp data for a sub plurality of flows; **(Column 18, Lines 28-42; Column 36, Lines 16-18; and Column**

37, Lines 5-12; The lookup table in Chao's system is the time stamp aging memory array.)

performing guaranteed aging processing steps for each flow utilizing the time stamp data subsets to identify and mark invalid calendar next time values **(Column 18, Lines 55-67; F_i is the calendar next time value for the i + 1 flow in Chao's system)**,

identifying a new frame arrival for an empty flow **(Figure 17, step 1740; Column 23, 1-20; Chao further shows in equation 14 that his system can differentiate between an empty and a non-empty flow)** and accessing time stamp data from a flow queue control block (FQCB) for the flow **(Figure 33 shows the time stamp aging memory (i.e. lookup table) and a flow control block for each flow as well as the flow time stamp. Column 36, Lines 60-67)** and the flow time stamp data in the time stamp aging memory array **(Column 18, Lines 26-41)**;

responsive to the identified new frame arrival for the empty flow, checking a selection indicator of the time stamp aging memory array data to identify the target calendar for attaching the flow; **(Chao's system is capable of identifying an empty flow and the arrival of a frame to such a flow as indicated in Figure 17, step 1740 and Column 23, Lines 1-20 and equation 14. In Chao's system the time stamp aging memory array is always accessed to read the target calendar (i.e. F_i). The selection indicator is inherent to Chao's system because his system supports different flows with different QoS and shaper-schedulers with different target calendar maintain these flows. See Column 13, Lines 15-21 and Column**

15, Lines 40-45. This indication along with any information deemed important to the session can be stored in the time stamp aging memory array. Column 18, Lines 35-37)

responsive to the selection indicator value, checking a target calendar next time valid bit of the time stamp aging memory array data for the flow **(Column 35, Lines 20-32)**;

responsive to the target calendar next time valid bit being on, comparing a target calendar next time from the flow queue control block (FQCB) for the flow with a current time**(In Chao's system the obsolete bit (See O_i in Figure 33) is the next time valid bit and if the calendar next time is not obsolete then it will be compared with current time. Column 36, Lines 53-67)**;

responsive to the target calendar next time being less than the current time, turning off the target calendar next time valid bit to mark the target calendar next time as invalid. **(Column 35, Lines 50-67 and Column 36, Lines 53-67; and Figure 33)**

4. Regarding **claim 2**, Chao discloses a scheduling method for implementing Quality-of-Service (QoS) scheduling of a plurality of flows with aging time stamps includes the steps of storing time stamp data for each flow in the flow queue control block (FQCB) and in the time stamp aging memory array **(Figure 33 shows the stamp aging memory array (i.e. lookup table) with a flow queue control block. See also Column 18, Lines 16-41 and Column 36, Lines 60-67)**; the flow queue control block (FQCB) for each flow stored in external static random access memory (SRAM) and the time stamp aging memory array stored in an internal scheduler memory array. **(Chao**

shows his is an improvement over previous systems internal memory on the chip housing the scheduler and his system uses off-chip memory. See Column 16, Lines 55-63)

5. Regarding **claim 3**, Chao discloses a scheduling method for implementing Quality-of-Service (QoS) scheduling of a plurality of flows with aging time stamps wherein the steps of storing time stamp data includes the steps of: identifying a flow for servicing on a calendar and dispatching a frame from the identified flow **(Figure 17, step 1710; Column 22, Lines 47-62)**;

calculating a calendar next time value for the identified flow **(Column 18, Lines 37-42)**;

and storing the calendar next time value for the identified flow in the flow queue control block (FQCB) for the identified flow **(Column 18, Lines 28-32 and Figure 33)**; and

storing time stamp data in the time stamp aging memory array**(Column 18, Lines 28-32 and Figure 33)**; the stored time stamp data in the time stamp aging memory array including at least a portion of the calendar next time value; the selection indicator and the calendar valid bit set to mark the calendar next time as valid. **(Column 36, Lines 60-67 and Figure 33)**

6. Regarding **claim 4**, Chao discloses a scheduling method for implementing Quality-of-Service (QoS) scheduling of a plurality of flows with aging time stamps wherein the guaranteed aging processing steps for each flow in the time stamp data subset include the steps of: checking the selection indicator, the selection indicator indicating a calendar **(A system like Chao's that supports different quality of service in each flow where shaper-schedulers maintain these flows has to have a**

selection indicator which can be stored in the FQCB. Column 13, Lines 15-21 and Column 15, Lines 40-45); responsive to the selection indicator, checking the calendar next time valid bit **(Column 35, Lines 20-32)**; responsive to the calendar next time valid bit being on, comparing a calendar next time with a current time **(Column 36, Lines 53-67;Figure 33)**;

and responsive to the calendar next time being less than the current time,

turning off the calendar next time valid bit to mark the calendar next time

as invalid **(Column 35, Lines 50-67 and Column 36, Lines 53-67, and Figure 33)**..

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 5-8 and 12-18** are rejected under 35 USC 103(a) as being unpatentable over Chao et al (US 6, 081, 507), hereinafter referred to as Chao, in view of Duckering et al (US 6, 721, 325), hereinafter referred to as Duckering.

9. Regarding **claims 5-8,** Chao teaches a scheduling method for implementing Quality-of-Service (QoS) scheduling of a plurality of flows with aging time stamps as discussed in the rejection of claims 1. Further Chao discloses a validity bit for the calendar time accessed from memory and if the bit is off the current time is used and if the bit is on then the next time calendar value belonging to the previous frame and

stored in memory is retrieved and used. **(Column 35, Lines 50-67 and Column 36, Lines 53-67, and Figure 33)**

Chao, however, fairs to expressly disclose that the different flows can be attached to different calendars such as Low Latency Service (LLS), Normal Latency Service (NLS), Peak Bandwidth Service (PBS), and Weighted Fair Queue (WFQ).

Duckering discloses a fair scheduling of multiple service classes with prioritized shaping. Duckering discloses an apparatus for scheduling a multi-service category ATM cell traffic through contention points in an ATM network is provided.

Duckering discloses a scheduling method for implementing Quality-of-Service (QoS) scheduling of a plurality of flows with aging time stamps wherein the target calendar can be PBS, LLS, NLS, and WFQ. **(First PBS, NLS, and LLS are simply quality of services that reflect traffic type, service category, and delay requirements for a particular Quality of Service. Duckering discloses the different quality of services that match PBS, NLS, and LLS and that are widely used in the art. Duckering further discloses traffic shapers using calendars based on these quality of services and also a WFQ calendar. See Figures 1, 2, and 3 and Column 4, Lines 1-35 and 57-67 and Column 5, Lines 10-21.)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chao's apparatus to incorporate a method of attaching to different calendars based on different QoS. The motivation is to provide different level of services with guaranteed QoS for each level while maintaining some form of fairness

which is the issue addressed by both Chao **(Column 13, Lines 15-21 and Column 15, Lines 40-45)** and Duckering **(Column 3, Lines 5-30)**.

10. Regarding **claims 12-18**, Chao teaches a scheduling method for implementing Quality-of-Service (QoS) scheduling of a plurality of flows with aging time stamps as discussed in the rejection of claims 1. Further Chao discloses a validity bit for the calendar time accessed from memory and if the bit is off the current time is used and if the bit is on then the next time calendar value belonging to the previous frame and stored in memory is retrieved and used. **(Column 35, Lines 50-67 and Column 36, Lines 53-67, and Figure 33)**

Chao, however, fairs to expressly disclose that the different flows can be attached to different calendars such as Low Latency Service (LLS), Normal Latency Service (NLS), Peak Bandwidth Service (PBS), and Weighted Fair Queue (WFQ).

Duckering discloses a scheduling method for implementing Quality-of-Service (QoS) scheduling of a plurality of flows with aging time stamps wherein the target calendar can be PBS, LLS, NLS, and WFQ. **(First PBS, NLS, and LLS are simply quality of services that reflect traffic type, service category, and delay requirements for a particular Quality of Service. Duckering discloses the different quality of services that match PBS, NLS, and LLS and that are widely used in the art. Duckering further discloses traffic shapers using calendars based on these quality of services and also a WFQ calendar. See Figures 1, 2, and 3 and Column 4, Lines 1-35 and 57-67 and Column 5, Lines 10-21.)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chao's apparatus to incorporate a method of attaching to different calendars based on different QoS. The motivation is to provide different level of services with guaranteed QoS for each level while maintaining some form of fairness which is the issue addressed by both Chao **(Column 13, Lines 15-21 and Column 15, Lines 40-45)** and Duckering **(Column 3, Lines 5-30)**.

11. **Claims 9-11 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao et al (US 6, 081, 507), hereinafter referred to as Chao, in view of Tayyar et al (US Pub. No. 2003/0050954), hereinafter referred to as Tayyar and in view of Duckering et al (US 6, 721, 325), hereinafter referred to as Duckering.

12. Regarding **claim 9**, Chao discloses a scheduler for implementing Quality-of-Service (QoS) scheduling of a plurality of flows with aging time stamps **(Column 1, Lines 15-20, Column 18, Lines 28-42)** comprising:

a time stamp aging memory array for storing a set of indicator bits and time stamp data for each of the plurality of flows **(Column 35, Lines 50-67 and Column 36, Lines 53-67, and Figure 33)**; the set of indicator bits including a calendar selector and at least one calendar next time valid bit **(Column 35, Lines 50-67 and Column 36, Lines 53-67, and Figure 33)**; a memory manager for sequentially accessing a subset of time stamp data from a time stamp aging memory array**(Since Chao's memory is an off-chip external RAM memory there has to be a memory manager)**; each time stamp data subset containing time stamp data for a sub plurality of flows **(See Figure 33)**; the memory manager for performing guaranteed aging processing steps for each flow in

each time stamp data subset to identify and mark invalid calendar next time values, queue manager for identifying a new frame arrival for an empty flow **(Column 35, Lines 20-32)**; the memory manager responsive to the new frame arrival for the empty flow for accessing time stamp data from a flow queue control block (FQCB) for the flow and the time stamp data in the time stamp aging memory array **(Figure 17, step 1740, Column 23, Lines 1-20)**; the memory manager responsive to the identified new frame arrival for the empty flow, for identifying a target calendar for attaching the flow **(Column 23, Lines 1-20);** the memory manager responsive to the identified target calendar, for checking the target calendar next time valid bit of the time stamp aging memory array data for the flow **(Column 36, Lines 53-67)**; the memory manager responsive to the target calendar next time valid bit being on, for comparing a target calendar next time value from the flow queue control block (FQCB) for the flow with a current time **(Column 36, Lines 53-67)**; the memory manager responsive to the target calendar next time being less than the current time, for turning off the target calendar next time valid bit to mark the target calendar next time as invalid **(Column 35, Lines 50-67 and Column 36, Lines 53-67, and Figure 33)**.

Chao, however, fails to expressly disclose the presence of a queue manager.

Tayyar discloses a weighted fair queuing scheduler.

Tayyar discloses a queue manager in his scheduling apparatus. Timestamper 18 in Figure 1 manages the queues. **(Column 3, Paragraph 44)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chao's apparatus to incorporate a queue manager.

The motivation is that Chao uses a weighted fair queuing scheduler with different queues associated with different QoS and the queues need to be managed and Tayyar provides a scheduler with a queue manager.

Chao also fails to expressly disclose the existence of different calendars.

Duckering teaches a scheduling method for implementing Quality-of-Service (QoS) scheduling of a plurality of flows with different calendars. **(See Figures 1, 2, and 3 and Column 4, Lines 1-35 and 57-67 and Column 5, Lines 10-21.)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chao's apparatus to incorporate a method of attaching to different calendars based on different QoS. The motivation is to provide different level of services with guaranteed QoS for each level while maintaining some form of fairness which is the issue addressed by both Chao **(Column 13, Lines 15-21 and Column 15, Lines 40-45)** and Duckering **(Column 3, Lines 5-30)**.

13. Regarding **claim 10**, Chao discloses a scheduler for implementing Quality-of-Service (QoS) scheduling of a plurality of flows with aging time stamps wherein the memory coupled to the queue manager for storing a flow queue control block (FQCB) for each of the plurality of flows includes an external static random access memory (SRAM). **(Chao shows his is an improvement over previous systems internal memory on the chip housing the scheduler and his system uses off-chip memory. See Column 16, Lines 55-63)**

14. Regarding **claim 11**, Chao discloses a scheduler for implementing Quality-of-Service (QoS) scheduling of a plurality of flows with aging time stamps wherein the

time stamp aging memory array includes an internal memory array. **(Chao shows his is an improvement over previous systems internal memory on the chip housing the scheduler and his** system **uses off-chip memory. See Column 16, Lines 55-63)**

15. Regarding **Claim 20**, Chao discloses a computer program product for implementing Quality-of-Service (QoS) scheduling of a plurality of flows with aging time stamps in a scheduler wherein the instructions, when executed by the scheduler, cause the scheduler to perform the steps of storing the flow queue control block (FQCB) for each of the plurality of flows in an external memory**(Column 18, Lines 28-32; Column 16, Lines 55-63 and Figure 33)**; and storing a set of indicator bits and time stamp data for each of the plurality of flows in a time stamp aging memory array, the set of indicator bits including the selector indicator and the calendar next time valid bit **(Column 36, Lines 60-67 and Figure 33)**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571 272 3088. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HM
08-19-2005

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